

# Analytical Modeling of Short-Channel Effects in BEOL-Compatible Thin-Film Transistors

Nilesh Pandey<sup>ID</sup>, *Member, IEEE*, Ujwal Radhakrishna<sup>ID</sup>, *Senior Member, IEEE*,  
Jian-Yu Lin<sup>ID</sup>, *Graduate Student Member, IEEE*, Chang Niu, *Member, IEEE*,  
Orlando Lazaro<sup>ID</sup>, *Member, IEEE*, Gianluca Boselli<sup>ID</sup>, *Senior Member, IEEE*,  
Luigi Colombo, *Fellow, IEEE*, Baher Haroun, *Life Fellow, IEEE*, Peide D. Ye<sup>ID</sup>, *Fellow, IEEE*,  
Leonard F. Register<sup>ID</sup>, *Life Fellow, IEEE*, and Sanjay K. Banerjee, *Life Fellow, IEEE*

**Abstract**—This article presents a 2-D analytical model for the potential and current characteristics of thin-film transistors (TFTs) using Green's function approach. The model accurately incorporates the effects of nonuniform trap charge distribution in the channel and includes both top and bottom gate oxide regions with different thicknesses. Solving 2-D Poisson's equation, we derive closed-form 2-D expressions for the potential profile in the channel. While the model applies to any thin-film technologies such as indium oxide ( $\text{In}_2\text{O}_3$ ), indium gallium zinc oxide (IGZO), graphene, carbon nanotubes (CNTs), etc., in this work, the model is validated using experimental data and TCAD Sentaurus simulations for  $\text{In}_2\text{O}_3$  TFTs. Key results include analysis of short-channel effects (SCEs), gate oxide scaling, and channel thickness variations on device performance. The model successfully predicts subthreshold characteristics and drain-induced barrier-lowering (DIBL) while identifying the limitations in the on current region due to the absence of various scattering phenomena, such as surface scattering in the analytical formulation. An improved mobility model, accounting for field dependence, enhances the accuracy in the on region, ensuring agreement with experimental and TCAD data across various bias conditions.

**Index Terms**—Green's function approach, indium oxide ( $\text{In}_2\text{O}_3$ ), thin-film transistors (TFTs).

## I. INTRODUCTION

THIN-FILM transistors (TFTs) were first reported in 1962 [1]. Subsequently, TFTs demonstrated remarkable applications in liquid-crystal displays [2], transparent indium gallium zinc oxide (IGZO) [3], and flexible

electronics [4], [5]. Recently, indium oxide ( $\text{In}_2\text{O}_3$ )-based TFTs have been extensively studied for back-end-of-line (BEOL) semiconductor manufacturing processes due to their compatibility with the atomic-layer-deposition (ALD) process, low thermal budget, and an expectantly high ON/OFF current ratio [6], [7], [8].

Chakraborty et al. [6] demonstrated the W-doped  $\text{In}_2\text{O}_3$  FET with  $I_{\text{ON}} \sim 370 \mu\text{A}/\mu\text{m}$ , and  $I_{\text{ON}}/I_{\text{OFF}} > 10^9$ . The ALD process has recently been used to fabricate TFTs with channel thickness  $\leq 1 \text{ nm}$  [7]. Exceptionally high ON current  $> 1 \text{ mA}/\mu\text{m}$  and mobility  $> 80 \text{ cm}^2/\text{V}\cdot\text{s}$  are observed in ALD-grown TFTs [9], [10]. Furthermore, monolithic 3-D integration of  $\text{In}_2\text{O}_3$  FETs is reported in [8] and [11].

The charge neutrality level (CNL) in intrinsic ( $\text{In}_2\text{O}_3$ ) resides well above the conduction band edge ( $E_c$ ) [12], [13]. Consequently, the Fermi level shifts toward the conduction band maximum, yielding a high electron density ( $10^{19}$ – $10^{20} \text{ cm}^{-3}$ ) even at zero bias [12], [14]. Oxygen vacancies act as shallow donors, making the channel inherently n-type. Since the trap density ( $N_t$ ) is directly linked to the electron density,  $N_t$  at equilibrium matches the carrier concentration. An increase in  $N_t$  effectively enhances n-type doping, reducing the barrier height. In contrast, in conventional n-p-n MOSFETs, higher channel doping raises the barrier height.

From a modeling perspective, the initial focus was on the amorphous silicon FET: A current–voltage and mobility model is presented by Shur et al. [15], and a SPICE-compatible circuit model in [16] and [17]. Recently, there have been reports on IGZO modeling aspects, such as current–voltage modeling above the threshold region in [18], 1-D surface potential modeling [19], [20], a drain current model including trap impact on [21], and a 1-D berkeley short-channel IGFET model (BSIM)-based TFT model in [22].

These modeling approaches can be broadly divided into two categories.

- 1) Surface-potential-based modeling, which considers 1-D Poisson's equation, incorporating only the gate-directional electric field into the surface potential modeling [17], [18], [19], [20]. The conformal mapping approach to obtain potential distribution is used in [23], and charge-based modeling is reported in [24].

Received 4 December 2024; revised 2 February 2025; accepted 25 February 2025. This work was supported in part by NSF National Nanotechnology Coordinated Infrastructure (NNCI) under Grant ECCS2025227. The review of this article was arranged by Editor B. Iñiguez. (Corresponding author: Nilesh Pandey.)

Nilesh Pandey, Leonard F. Register, and Sanjay K. Banerjee are with the Microelectronics Research Center, The University of Texas at Austin, Austin, TX 78703 USA (e-mail: pandey@utexas.edu; register@austin.utexas.edu; banerjee@ece.utexas.edu).

Ujwal Radhakrishna, Orlando Lazaro, Gianluca Boselli, Luigi Colombo, and Baher Haroun are with Kilby Labs Texas Instruments Inc., Dallas, TX 75243 USA.

Jian-Yu Lin, Chang Niu, and Peide D. Ye are with the School of Electrical and Computer Engineering, Purdue University, West Lafayette, IN 47907 USA.

Digital Object Identifier 10.1109/TED.2025.3546593

## 2) SPICE-compatible circuit modeling based on 1-D Poisson's equation [16], [17], [22].

However, none of these models incorporates 2-D Poisson's equation to obtain the potential distribution in the channel, which has a 2-D spatial dependence  $(x, y)$ . Solving 2-D Poisson's equation is necessary to accurately capture the impact of oxide/channel scaling on threshold voltage roll-off and drain-induced barrier-lowering (DIBL) [25], [26], [27], [28], [29]. Furthermore, 1-D Poisson's equation only considers the gate-directed electric field (in the  $y$ -direction), neglecting the drain-to-source electric field, which means it cannot capture short-channel effects (SCEs) [25], [27]. Solution to 2-D Poisson's equation is required to predict threshold voltage roll-off, subthreshold slope degradation, and DIBL, which are crucial for studying device (technology) scaling analysis.

Therefore, this work focuses on the 2-D analytical modeling of TFTs, including the impact of the gate and drain electric fields in deriving the 2-D channel potential. The derived model can predict the impact of scaling of physical parameters such as oxide thickness, channel thickness, and channel length on the device's SCEs and DIBL.

Fundamentally, there are two analytical approaches available in the literature to solve 2-D Poisson's equations: 1) scale-length modeling [25] and 2) Green's function approach [26]. Both the models are consistent with TCAD. However, the scale-length model cannot handle a nonuniform doping profile in the channel [26]. On the other hand, the scale-length model requires fewer terms than Green's function approach. Since TFTs have trap charges in the channel, which possess a 2-D spatial distribution, this work adapts Green's function approach to model the SCEs in TFTs [26].

The 2-D analytical model provides deeper insights into device physics, as the potential equation directly reveals first-order approximations of how physical parameter scaling impacts the electrostatic barrier. In addition, we simplify the analytical model into a unified potential equation (54). The surface potential at the mid-channel can be obtained by setting  $x = L/2$  and  $y = t_{ox1}$ , which serves as a foundation for circuit-level or SPICE-level modeling. A key advantage of the analytical model over TCAD simulations is its computational efficiency. It generates  $I_d$ - $V_g$  curves within seconds, whereas TCAD simulations can take significantly longer depending on the setup. Furthermore, the analytical model always converges due to its compact formulation, whereas TCAD simulations can face convergence challenges.

## II. TRAP PROFILE MODELING

Fig. 1 shows the schematic of the double-gate thin film transistor considered in this work with different top and bottom gate oxide thicknesses. The 2-D trap distribution can be analytically modeled as

$$\rho(x, y) = f(x)f(y). \quad (1)$$

The  $\text{In}_2\text{O}_3$  material exhibits bulk trap density [12], [13], leading to  $f(y) = qN_t/\epsilon$ , where  $q$ ,  $N_t$ , and  $\epsilon$  are the electron charge, peak value of trap concentration (constant), and channel permittivity, respectively.

The function  $f(x)$  includes the variation in the trap distribution along the  $x$ -direction [source to drain direction (S-D)].

Authorized licensed use limited to: Purdue University. Downloaded on March 13, 2025 at 20:21:30 UTC from IEEE Xplore. Restrictions apply.

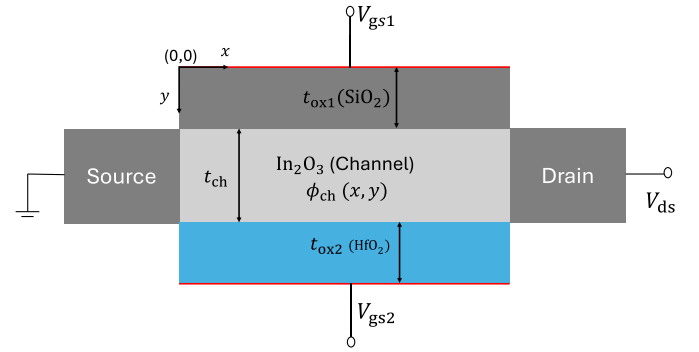


Fig. 1. Schematic of  $\text{In}_2\text{O}_3$  TFT. Default parameters: Channel thickness ( $t_{ch} = 1$  nm), back-gate oxide thickness ( $t_{ox2} = 5$  nm), front-gate oxide thickness ( $t_{ox1} = 4$  nm), channel length ( $L = 40$  nm), drain bias ( $V_{ds} = 0.5$  V), top gate voltage ( $V_{gs1} = 0$  V),  $\text{SiO}_2$  relative permittivity = 3.9, and  $\text{HfO}_2$  relative permittivity = 15.

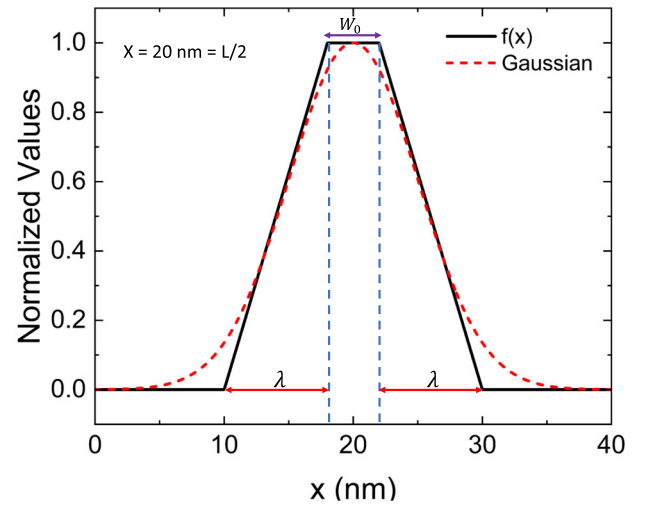


Fig. 2. Comparison between approximated and Gaussian trap profile in the channel. Default parameters:  $\lambda = 8$  nm,  $W_0 = 4$  nm, and peak trap density =  $1 \times 10^{20} \text{ cm}^{-3}$ .

In general, for numerical modeling purposes, it is reasonable to assume the Gaussian trap distribution [29], [30], [31]. Furthermore, the model validation section shows that assuming Gaussian trap distribution leads to model consistency with the experimental and TCAD data. However, an exact Gaussian function will not produce analytical solutions for 2-D Poisson's equation. Since this work aims to derive an analytical model, it is imperative to approximate the Gaussian distribution in a closed-form equation. Fig. 2 shows comparison of the approximated function  $f(x)$  and the exact Gaussian function.

The function  $f(x)$  is defined in the Fourier series form

$$f(x) = \frac{a_0}{2} + \sum_j A_j \cos(k_j x). \quad (2)$$

Note that there will not be sine terms in (2) due to the even symmetry of the function  $f(x)$ . Here,  $a_0$  is the zero-order Fourier series coefficient,  $T_D$  is the period, and  $A_j$  is the  $j$ th series coefficient, calculated below

$$a_0 = \frac{2}{T_D} \int_{T_D} f(x) dx = \left( \frac{2}{T_D} \right) (\lambda + W_0) \quad (3)$$

$$A_j = \frac{2}{T_D} \int_{T_D} \cos(k_j x) f(x) dx$$

$$= \frac{1}{\lambda} \left( \frac{\cos(k_j x_b) - \cos(k_j x_a)}{k_j^2} + \frac{\lambda \sin(k_j x_b)}{k_j} \right) + \frac{1}{\lambda} \left( \frac{\cos(k_j x_c) - \cos(k_j x_d)}{k_j^2} - \frac{\sin(k_j x_c)}{k_j} \right) + \frac{\sin(k_j x_c) - \sin(k_j x_b)}{k_j} \quad (4)$$

$$x_a = L/2 - W_0/2 - \lambda; \quad x_b = L/2 - W_0/2; \quad (5)$$

$$x_c = L/2 + W_0/2; \quad x_d = L/2 + W_0/2 + \lambda$$

$$T_D = 2\lambda + W_0 + k_0 L; \quad k_j = \frac{2\pi j}{T_D} \quad (6)$$

where  $k_0 > 1$  ensures that the function  $f(x)$  does not repeat in the channel twice, signifying a correct distribution function (see Fig. 2).

### III. 2-D ANALYTICAL POTENTIAL PROFILE MODELING

The 2-D Poisson's equation in the oxide and channel regions can be expressed as

$$\frac{\partial^2 \phi_1^{\text{ox}}(x, y)}{\partial x^2} + \frac{\partial^2 \phi_1^{\text{ox}}}{\partial y^2} = 0 \quad [\text{Top oxide}] \quad (7)$$

$$\frac{\partial^2 \phi(x, y)}{\partial x^2} + \frac{\partial^2 \phi(x, y)}{\partial y^2} = \rho(x, y) \quad [\text{Channel}] \quad (8)$$

$$\frac{\partial^2 \phi_2^{\text{ox}}(x, y)}{\partial x^2} + \frac{\partial^2 \phi_2^{\text{ox}}}{\partial y^2} = 0 \quad [\text{Bottom oxide}]. \quad (9)$$

We consider a generic device with different top and gate oxide thicknesses as  $t_{\text{ox1}}$  and  $t_{\text{ox2}}$ , respectively, as well as materials with different permittivities. The model will also apply to symmetric cases by replacing  $t_{\text{ox1}} = t_{\text{ox2}} = t_{\text{ox}}$ .

Green's identity is a well-established method for obtaining analytical closed-form solutions to electrostatics boundary-value problems, which can handle nonuniform charge distribution in 2-D Poisson's equation [26], [32]. In a bounded region, Green's identity is expressed as

$$\phi(x, y) = \int \int \left( \frac{\rho(x', y')}{\epsilon} \right) G(x, y; x', y') dx' dy' + \oint_l \left\{ G(x, y; x', y') \frac{\partial \phi}{\partial n'} - \phi \frac{\partial G(x, y; x', y')}{\partial n'} \right\} dl'. \quad (10)$$

The first step is to derive Green's functions  $[G(x, y; x', y')]$  for the various regions using the Dirichlet and Neumann boundary conditions. A detailed methodology for calculating Green's functions is provided in our earlier work [33]. The following potential profiles are obtained by substituting Green's functions into Green's identity.

#### A. Channel Region

The impact of trap charge distribution on the potential profile is primarily included in the first term of (10). For  $n \neq 0$ , substituting the channel region Green's function (60) into (10) results in a zero value due to the cosine integration term

$$\int_{t_{\text{ox1}}}^{t_{\text{ox1}}+t_{\text{ch}}} \cos \left[ \frac{n\pi(t_{\text{ox1}} + t_{\text{ch}} - y')}{t_{\text{ch}}} \right] dy' = 0.$$

Green's function for the  $n = 0$  term is calculated as

$$G_y^{II}(x, y; x', y')_{n=0} = \frac{1}{t_{\text{ch}} L} \begin{cases} (L - x')x & 0 < x < x' \\ x'(L - x) & x' < x < L \end{cases}. \quad (11)$$

Using (11) in (10), we derive the following potential profile:

$$\phi_{\text{trap}}(x) = N_t(L - x) \int_0^{x'} x' f(x') dx' + N_t x \int_{x'}^L (L - x') f(x') dx'. \quad (12)$$

Substituting  $f(x)$  from (2) into (12) and simplifying

$$\phi_{\text{trap}}(x) = \frac{2}{T_D} \left( \frac{q N_t}{\epsilon L} \right) \frac{a_0}{4} L x (L - x) + \frac{2}{T_D} \left( \frac{q N_t}{\epsilon L} \right) \left\{ \sum_j \frac{A_j (L \cos(k_j x) - x \cos(k_j L) + x - L)}{k_j^2} \right\}. \quad (13)$$

Top gate oxide and bottom gate oxide interfaces exhibit the Neumann boundary conditions. Hence, the second term from (10) derives the following potential function at the top and bottom interfaces:

$$\phi^{T,B}(x, y) = \oint_l G(x, y; x', y') \frac{\partial \phi}{\partial n'} dl'. \quad (14)$$

Plugging Green's function (59) into the above equation

$$\phi^{T,B}(x, y) = \frac{2}{L} \sum_m \frac{\sin(k_m x)}{k_m \epsilon \sinh(k_m t_{\text{ch}})} \times \{ D_{sf} \cosh(k_m(t_{\text{ox1}} + t_{\text{ch}} - y)) - D_{sb} \cosh(k_m(t_{\text{ox1}} - y)) \} \quad (15)$$

where  $k_m = m\pi/L$ ,  $D_{sf}$ , and  $D_{sb}$  are the Fourier coefficients for the top and bottom interfaces, respectively, defined as

$$D_{sf} = -\epsilon \int_0^L \sin(k_m x') \frac{\partial \phi}{\partial y'} dx' \quad \text{at } y = t_{\text{ox1}} \quad (16)$$

$$D_{sb} = -\epsilon \int_0^L \sin(k_m x') \frac{\partial \phi}{\partial y'} dx' \quad \text{at } y = t_{\text{ox1}} + t_{\text{ch}}. \quad (17)$$

The left and right boundary interfaces,  $x = 0$  and  $x = L$ , exhibit the Dirichlet boundary conditions, leading to the following potential profile:

$$\phi^{L,R}(x, y) = - \oint_l \phi(x, y) \frac{\partial G(x, y; x', y')}{\partial n'} dl'. \quad (18)$$

Using Green's function (60) in the above equation

$$\phi^{L,R}(x, y) = \frac{2}{t_{\text{ch}}} \sum_n \frac{\cos(k_n''(t_{\text{ox1}} + t_{\text{ch}} - y))}{\sinh(k_n'' L)} \times (B_s^n \sinh(k_n''(L - x)) + B_d^n \sinh(k_n'' x)). \quad (19)$$

Here,  $k_n'' = n\pi/t_{\text{ch}}$ ,  $B_{ns}$ , and  $B_{nd}$  are the left and right boundaries' Fourier series coefficients. All the necessary series coefficients are derived in Section IV. The net potential equation in the channel is followed as:

$$\phi_{\text{ch}}(x, y) = \phi_{\text{trap}}(x) + \phi^{T,B}(x, y) + \phi^{L,R}(x, y). \quad (20)$$

### B. Top Gate Oxide Region

Oxide regions do not have any free charge. Hence,  $\rho(x, y) = 0$ . Due to the known applied voltage  $V_{gs1}$ , the top interface is at the Dirichlet boundary condition. Plugging (58) into Green's identity and simplifying

$$\begin{aligned} \phi_{ox_1}^T(x, y) &= \int_0^L \phi_{ox_1}^T(x, y)(x', 0) \left( \frac{\partial G_x^I}{\partial y'} \right)_{y>y'} dx' \\ &= \frac{2}{L} \sum_m \frac{\sin(k_m x) \cosh(k_m(t_{ox_1} - y)) V_1 (1 + (-1)^{m+1})}{k_m \cos(k_m t_{ox_1})}. \end{aligned} \quad (21)$$

Here,  $V_1 = V_{gs1} - V_{fb}$ , and  $V_{fb}$  is the flat band voltage.

The interface along the oxide/channel (or bottom interface of the top gate oxide region) uses the Neumann boundary condition, using  $G_x^I$  into (10) with  $y = t_{ox_1}$

$$\begin{aligned} \phi_{ox_1}^B(x, y) &= \oint_l G(x, y; x', y') \frac{\partial \phi}{\partial y'} dx' \\ \phi_{ox_1}^B(x, y) &= -\frac{2}{L} \sum_m \frac{\sin(k_m x) \sinh(k_m y) D_{sf}}{k_m \epsilon_{ox_1} \cosh(k_m t_{ox_1})}. \end{aligned} \quad (22)$$

The left and right interfaces are at the Dirichlet boundary conditions since these gap potentials can be approximated as the linear profile [26]. Using (57) in (10), and simplifying

$$\begin{aligned} \phi_{ox_1}^{L,R}(x, y) &= \frac{2}{t_{ox_1}} \sum_n \frac{\sin(k_n^I y)}{\sinh(k_n^I L)} \\ &\times (A_s^n \sinh(k_n^I(L - x)) + A_d^n \cdot \sinh(k_n^I x)) \end{aligned} \quad (23)$$

where,  $k_n^I = (2n - 1)\pi/t_{ox_1}$ .

### C. Bottom Gate Oxide Region

Since the top and bottom gate oxide thicknesses are different, leading to  $D_{sf} \neq -D_{sb}$ , we follow a similar approach used for the top gate oxide region to derive the potential function of the bottom gate oxide region:

$$\begin{aligned} \phi_{ox_2}(x, y) &= \frac{2}{L} \sum_m \frac{\sin(k_m x) D_{sb} \sinh(k_m(t_0 - y))}{\epsilon_{ox_2} k_m \cos(k_m t_{ox_2})} \\ &+ \frac{2}{L} \sum_m \frac{\sin(k_m x) \cosh(k_m(t_1 - y)) V_2 (1 + (-1)^{m+1})}{k_m \cos(k_m t_{ox_2})} \\ &+ \frac{2}{t_{ox_2}} \sum_n \frac{\sin(k_n^{III}(t_0 - y))}{\sinh(k_n^{III} L)} \\ &\times (C_s^n \sinh(k_n^{III}(L - x)) + C_d^n \sinh(k_n^{III} x)) \end{aligned} \quad (24)$$

where,  $t_0 = t_{ox_1} + t_{ch} + t_{ox_2}$ , and  $k_n^{III} = \frac{(2n-1)\pi}{t_{ox_2}}$ .

## IV. FOURIER SERIES COEFFICIENTS CALCULATION

The coefficients  $D_{sf}$  and  $D_{sb}$  are defined such that electric displacement continuity is maintained at the oxide/channel interface [26]. The next step is to ensure potential continuity

at the interfaces, after which  $D_{sf}$  and  $D_{sb}$  are determined using standard Fourier series coefficient calculations [26]

$$\int_0^L \phi_{ox_1}(x, t_{ox_1}) \sin(k_m x) dx = \int_0^L \phi_{ch}(x, t_{ox_1}) \sin(k_m x) dx \quad (25)$$

$$\int_0^L \phi_{ch}(x, t_1) \sin(k_m x) dx = \int_0^L \phi_{ox_1}(x, t_1) \sin(k_m x) dx \quad (26)$$

where,  $t_1 = t_{ox_1} + t_{ch}$ , and  $t_2 = t_1 + t_{ox_2}$ . Solving the above two equations for  $D_{sf}$  and  $D_{sb}$

$$D_{sf} = \frac{d_\lambda d_0^m - d_\gamma d_1^m}{(d_0^m)^2 - d_2^m d_1^m} \quad (27)$$

$$D_{sb} = \frac{d_\lambda d_2^m - d_\gamma d_0^m}{(d_0^m)^2 - d_2^m d_1^m} \quad (28)$$

$$d_\gamma = d_3^m + d_4^{m,n} - d_5^{m,n} - d_{trap} \quad (29)$$

$$d_\lambda = d_6^{m,n} + d_7^{m,n} + d_8^m - d_{trap} \quad (30)$$

$$d_{trap} = \frac{2}{T_D} \left( \frac{q N_t}{\epsilon L} \right) \sum_j \frac{A_j}{k_j^2} (d_a^{m,j} + d_b^{m,j}) \quad (31)$$

$$d_a^{m,j} = L(1 + (-1)^{m+1} \cos(k_j L)) \left( \frac{k_m}{k_m^2 - k_j^2} - \frac{1}{k_m} \right) \quad (32)$$

$$d_b^{m,j} = \frac{(\lambda + W_0)L(1 + (-1)^{m+1})}{4} \quad (33)$$

$$d_0^m = \frac{1}{\epsilon k_m \sinh(k_m t_{ch})} \quad (34)$$

$$d_1^m = \frac{1}{\epsilon k_m \tanh(k_m t_{ch})} + \frac{\tanh(k_m t_{ox_2})}{k_m \epsilon_{ox_2}} \quad (35)$$

$$d_2^m = \frac{1}{\epsilon k_m \tanh(k_m t_{ch})} + \frac{\tanh(k_m t_{ox_1})}{k_m \epsilon_{ox_1}} \quad (36)$$

$$d_3^m = \frac{V_1(1 + (-1)^{m+1})}{k_m \cosh(k_m t_{ox_1})} \quad (37)$$

$$d_4^{m,n} = \frac{2}{t_{ox_1}} \sum_n \frac{\sin(k_n^I t_{ox_1}) k_m (A_s^n + A_d^n (-1)^{m+1})}{k_m^2 + (k_n^I)^2} \quad (38)$$

$$d_5^{m,n} = \frac{2}{t_{ch}} \sum_n \frac{\cos(k_n^{II} t_{ch}) k_m (B_s^n + B_d^n (-1)^{m+1})}{k_m^2 + (k_n^{II})^2} \quad (39)$$

$$d_6^{m,n} = \frac{2}{t_{ox_2}} \sum_n \frac{\sin(k_n^{III} t_{ox_2}) k_m (C_s^n + C_d^n (-1)^{m+1})}{k_m^2 + (k_n^{III})^2} \quad (40)$$

$$d_7^{m,n} = \frac{2}{t_{ch}} \sum_n \frac{(B_s^n + B_d^n (-1)^{m+1}) k_m}{k_m^2 + (k_n^{II})^2} \quad (41)$$

$$d_8^m = \frac{V_2(1 + (-1)^{m+1})}{k_m \cosh(k_m t_{ox_2})}. \quad (42)$$

The boundary gaps ( $x = 0/L$ ) Fourier coefficients are calculated by assuming a linear potential profile, a valid approximation consistent with the TCAD [26]. Along line  $x = 0$ , the following linear potential profiles can be written in the various regions:

$$\begin{aligned} \phi_{ox_1}(0, y') &= c_1 y' + c_2; \quad \phi_{ch}(0, y') = c_3 y' + c_4 \\ \phi_{ox_2}(0, y') &= c_5 y' + c_6 \end{aligned} \quad (43)$$



where  $c_1, c_2, c_3, c_4, c_5$ , and  $c_6$  are the constants calculated by the boundary conditions

$$\phi_{\text{ox}_1}(0, 0) = V_1 \quad (44)$$

$$\phi_{\text{ox}_1}(0, t_{\text{ox}_1}) = \phi_{\text{ch}}(0, t_{\text{ox}_1}) \quad (45)$$

$$\phi_{\text{fe}}(0, t_{\text{ox}_1} + t_{\text{ch}}) = \phi_{\text{ox}_2}(0, t_{\text{ox}_1} + t_{\text{ch}}) \quad (46)$$

$$\phi_{\text{ox}_2}(0, t_{\text{ox}_1} + t_{\text{ch}}) = V_2 \quad (47)$$

$$-\epsilon(c_3) + \sigma(0, t_{\text{ox}_1}) = -\epsilon_{\text{ox}_1}(c_1) \quad (48)$$

$$-\epsilon(c_3) + \sigma(0, t_{\text{ox}_1} + t_{\text{ch}}) = -\epsilon_{\text{ox}_2}(c_5). \quad (49)$$

$\sigma(0, t_{\text{ox}_1}) = \sigma(0, t_{\text{ox}_1} + t_{\text{ch}}) = N_t \times (t_{\text{ch}})$  is the surface trap concentration. Subsequently, the series coefficients are calculated as

$$\begin{aligned} A_n^s &= \int_0^{t_{\text{ox}_1}} \phi_{\text{ox}_1}(0, y') \sin(k_n^I y') dy' \\ &= \frac{V_1}{k_n^I} + c_1 \frac{\sin(k_n^I t_{\text{ox}_1})}{(k_n^I)^2} \end{aligned} \quad (50)$$

$$\begin{aligned} B_n^s &= \int_{t_{\text{ox}_1}}^{t_1} \phi_{\text{ch}}(0, y') \cos(k_n^{II}(t_1 - y')) dy' \\ &= c_3 \frac{1 + (-1)^{n+1}}{(k_n^{II})^2} \end{aligned} \quad (51)$$

$$\begin{aligned} C_n^s &= \int_{t_1}^{t_2} \phi_{\text{ox}_2}(0, y') \sin(k_n^{III} y') dy' \\ &= c_5 \left( \frac{t_{\text{ox}_2}}{k_n^{III}} + \frac{(-1)^n}{(k_n^{III})^2} \right) + \frac{c_6}{k_n^{III}} \end{aligned} \quad (52)$$

where  $t_1 = t_{\text{ox}_1} + t_{\text{ch}}$  and  $t_2 = t_{\text{ox}_1} + t_{\text{ch}} + t_{\text{ox}_2}$ .

## V. SIMPLIFIED CHANNEL POTENTIAL MODEL

The analytical model is derived for a double-gate (DG) TFT where the body is not grounded. Therefore, the electrostatic boundary conditions closely resemble those of silicon-based DG-MOSFET [26]. Hence, the channel's gap potential can be approximated similar to the reports for DG-MOSFET [26], [27] as

$$\phi_{\text{ch}}(0, y) = \frac{E_g}{2q}, \quad \text{and} \quad \phi_{\text{ch}}(L, y) = \frac{E_g}{2q} + V_{\text{ds}}. \quad (53)$$

The above approximation significantly simplifies the mathematics by forcing

$$d_5^{m,n} = d_7^{m,n} = 0.$$

The channel potential is expressed as

$$\phi_{\text{ch}}(x, y) = \frac{E_g}{2q} + \frac{x}{L} V_{\text{ds}} + \phi^{T,B}(x, y) + \phi_{\text{trap}}(x). \quad (54)$$

Fig. 3 shows a comparison between the exact potential model (20) and the approximate model (54). The approximate channel potential model accurately captures the barrier height, which is the primary factor in the subthreshold region.

Furthermore, the calculation of boundary gaps Fourier coefficients is also simplified: for  $A_n^s, B_n^s$ , and  $C_n^s$ ,  $\phi_{\text{ch}}(0, y') = \frac{E_g}{2q}$ , and for  $A_n^d, B_n^d$ , and  $C_n^d$ ,  $\phi_{\text{ch}}(L, y') = \frac{E_g}{2q} + V_{\text{ds}}$  is used.

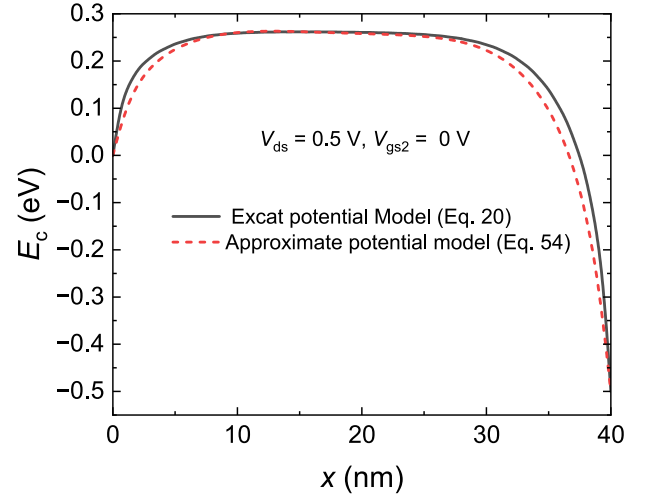


Fig. 3. Comparison between exact potential model [see 20] and approximate potential model [see 54]. Even with the approximation, maximum barrier height is predicted correctly, leading to a correct prediction in the OFF current.

## VI. MODEL VALIDATION

### A. Constant Mobility Drain Current Model

The current equation in the channel is derived by following the current continuity equation [26]:

$$I_{\text{ds}} = \frac{q\mu W V_t n_i (1 - \exp(-V_{\text{ds}}/V_t))}{\int_0^L \frac{dx}{\int_{t_{\text{ox}_1}}^{t_{\text{ox}_1} + t_{\text{ch}}} \exp(\phi_{\text{ch}}(x, y)/V_t) dy}} \quad (55)$$

where  $q$  is the electron charge,  $\mu$  is the constant mobility =  $9 \text{ cm}^2/\text{V}\cdot\text{s}$ ,  $W$  is the device width =  $1 \text{ }\mu\text{m}$ ,  $V_t$  is the thermal voltage, and  $V_{\text{ds}}$  is the drain bias. The intrinsic charge density  $n_i = 5 \times 10^{19} \text{ cm}^{-3}$ , consistent with typical observations in undoped  $\text{In}_2\text{O}_3$  material [12], [14].

Fig. 4 presents the validation of the developed model against experimental and TCAD data. The  $\text{In}_2\text{O}_3$  TFT was fabricated and measured at Purdue University, with the experimental data collected in collaboration with Texas Instruments. The TCAD Sentaurus simulations were first calibrated using the experimental data. The key parameters for the TCAD setup are as follows.

- 1) The trap concentration in the channel is  $1 \times 10^{20} \text{ cm}^{-3}$ , located 0.4 eV above the conduction band edge.
- 2) The trap density in the source and drain is  $4 \times 10^{20} \text{ cm}^{-3}$ .
- 3) A Gaussian trap distribution is assumed along the source-drain direction.
- 4) The mobility model includes surface scattering, phonon scattering, and high-field saturation effects.

Fig. 4(a) shows comparison of the analytical model with the experimental and TCAD data for  $V_{\text{ds}} = 0.5 \text{ V}$ . While the analytical model with constant mobility accurately captures the subthreshold region, it underpredicts the ON current. This is expected because the inversion charge density in the channel has not been incorporated into the solution of 2-D Poisson's equation (8). Including the inversion charge density in the analytical solution is complex and outside the scope of this work [26].

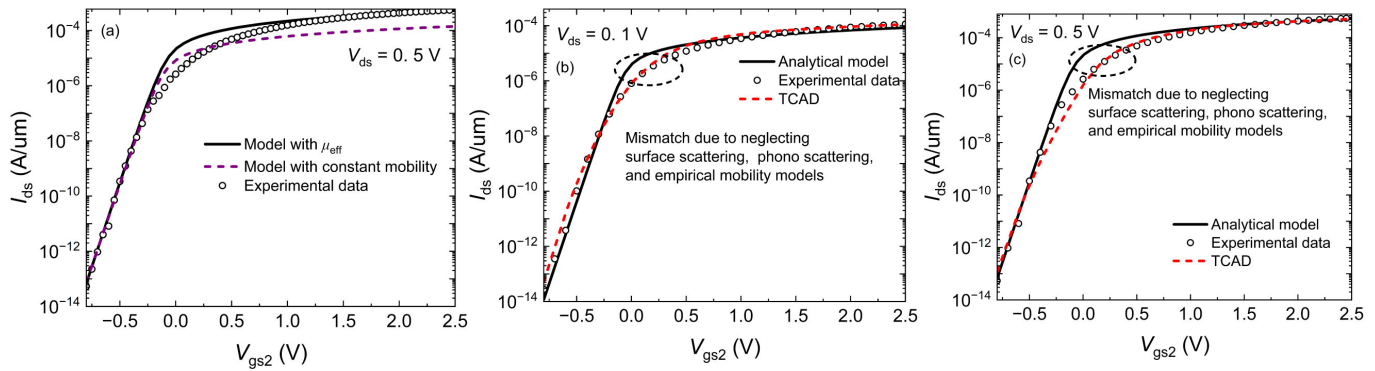


Fig. 4. (a) Field-dependent mobility model improves the ON region matching. (b) and (c) Validation of the analytical model for low and high drain voltages with the experimental data and calibrated TCAD deck with  $V_{gs1} = 0$  V. Default parameters are taken from Fig. 1.

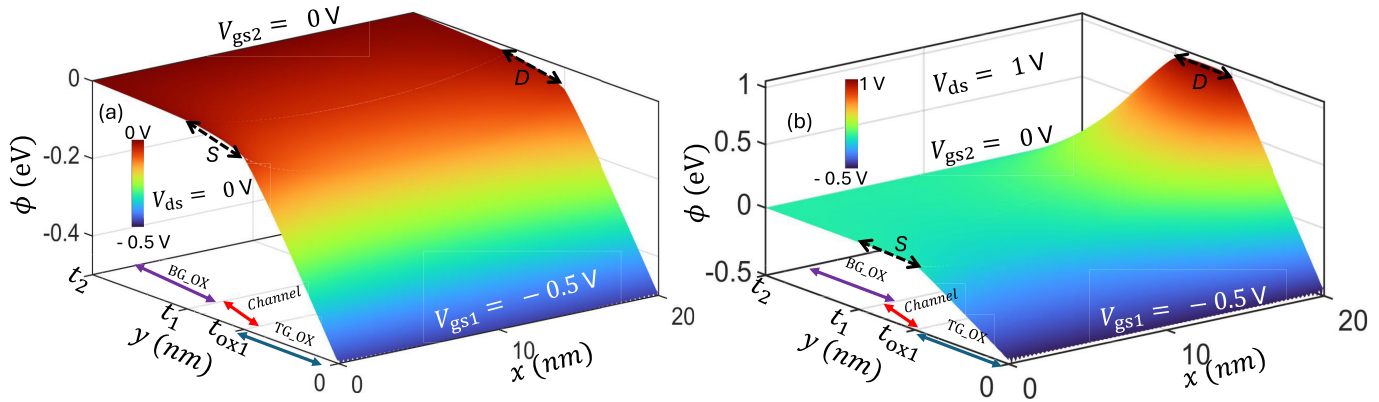


Fig. 5. (a) and (b) 3-D surface potential distribution in the device for  $V_{ds} = 0$  V, and  $V_{ds} = 1$  V, respectively. Note that potential continuity is maintained at both top oxide/channel interfaces. For  $V_{ds} = 1$  V, the highest potential drop is observed near the drain region following the applied bias condition. (a) Parameters:  $V_{gs1} = -0.5$  V and  $V_{gs2} = 0$  V. The source side potential is taken as a reference point, i.e.,  $= 0$  V.

## VII. RESULTS AND DISCUSSION

### A. Improved Mobility Model

The constant mobility model tends to underestimate the ON current. To address this, an analytical mobility model is used, where mobility increases with gate bias and saturates at higher values, similar to current saturation. A robust and straightforward approach to deriving such a model is through a hyperbolic function, which provides a smooth transition and ensures physical accuracy. The effective mobility is derived

$$\mu_{\text{eff}} = \mu_0(1 + \tanh(V_g - V_0)) \quad (56)$$

where  $\mu_0 = 7.2$  cm<sup>2</sup>/V-s, and  $V_0$  is the minimum applied gate voltage. With the updated mobility model, the analytical model shows consistency in the ON region, as demonstrated in Fig. 4(a). Fig. 4(b) and (c) further validates the analytical model against experimental data for both low and high drain voltages, incorporating the improved mobility model.

However, due to the limitations of the analytical approach, it is not feasible to incorporate extensive empirical mobility models or account for effects such as surface scattering and phonon scattering. As a result, some discrepancies are observed between the analytical model in the moderate inversion region. It is important to note that this work is not primarily focused on modeling the ON current region in the TFTs. Nonetheless, we have enhanced the mobility model to reflect

the requirement for BEOL TFTs to operate effectively as current drivers, where the ON current plays a crucial role.

*Note:* The model is validated for a gate length of  $L = 40$  nm. While validation across multiple gate lengths would further assess the model's robustness, we limit our validation to a single gate length due to data availability. However, the calculated subthreshold swing (SS) and threshold voltage roll-off as a function of channel length scaling align with physical expectations, demonstrating the model's capability to capture SCEs accurately.

Fig. 5(a) and (b) shows the 3-D surface potential distribution for the entire device for  $V_{ds} = 0$  V, and  $V_{ds} = 1$  V, respectively. The top and bottom gates are at  $-0.5$  and  $0$  V, respectively. The potential continuity is maintained at the bottom and top gate oxide with the channel interface, including the impact of drain bias, signifying the model's accuracy.

Fig. 6 presents the conduction band profile at the back-gate oxide and channel interface. The analytical model effectively predicts the maximum barrier height in the channel, accurately capturing the DIBL effect.

Fig. 7 shows the  $I_{ds} - V_{gs}$  characteristics for various gate oxide thicknesses at  $L = 15$  and  $40$  nm. Increasing the gate oxide thickness weakens the gate control over the channel, leading to an increase in the OFF current value. Furthermore, due to the reduced gate capacitance, the ON current also decreases at higher gate oxide thickness.

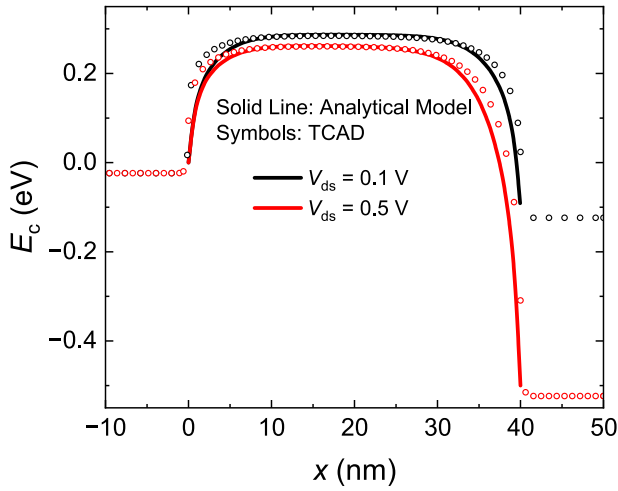


Fig. 6. Electrostatic conduction band validation with the TCAD. The model accurately captures the maximum barrier height and DIBL effect. Default parameters from Fig. 1.

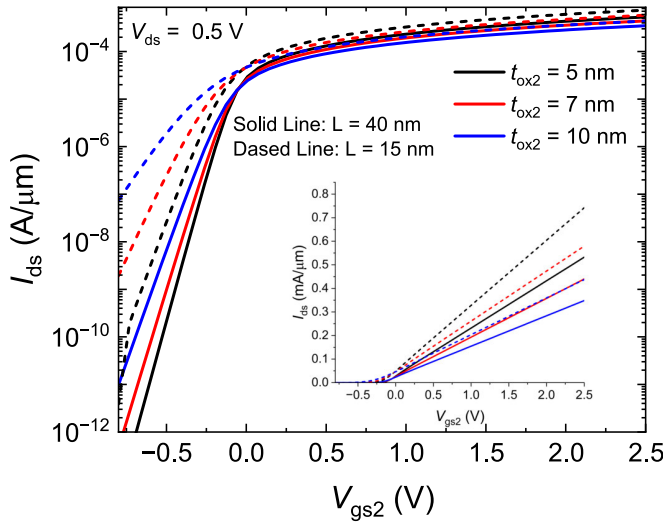


Fig. 7. Impact of oxide thickness scaling on SCEs and threshold voltage roll-off. A higher gate oxide thickness reduces the gate control and increases the OFF current. Default parameters are taken from Fig. 1. Default parameters are taken from Fig. 1.

A comparison between  $L = 15$  and  $40$  nm provides insight into threshold voltage roll-off. The gate voltage required to achieve a current level of  $1 \text{ nA}/\mu\text{m}$  at  $t_{\text{ox}2} = 5 \text{ nm}$  is approximately  $-0.3959 \text{ V}$  for  $L = 40 \text{ nm}$  and  $-0.5976 \text{ V}$  for  $L = 15 \text{ nm}$ , resulting in a reduction of approximately  $200 \text{ mV}$  in  $V_{\text{th}}$ . This threshold voltage roll-off increases to approximately  $630 \text{ mV}$  for  $t_{\text{ox}2} = 10 \text{ nm}$ . Therefore, the device's electrostatic integrity diminishes significantly with increasing oxide thickness and shorter channel lengths.

Fig. 8 shows the impact of channel length scaling on the SCEs and  $I_{\text{ON}}$ . Severe SCEs are observed for  $L = 15 \text{ nm}$ , while increasing the channel length improves gate control by reducing the influence of the drain electric field. The long-channel limit is observed around  $L = 80 \text{ nm}$ . Beyond this gate length, saturation in the OFF current is observed due to the long-channel barrier height, which is not affected by the channel length modulation.

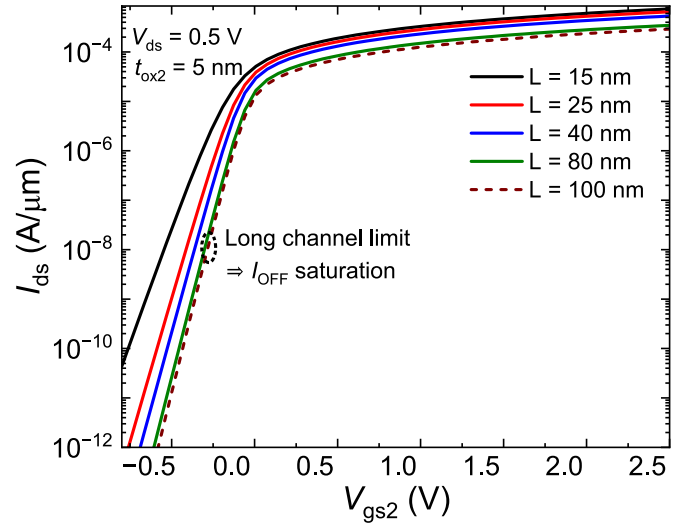


Fig. 8. Impact of channel length scaling on the device's threshold voltage roll-off. The increasing channel length weakens the drain electric field control on the channel, enhancing the gate control. The long channel limit is  $\sim 80 \text{ nm}$ . Default parameters are taken from Fig. 1.

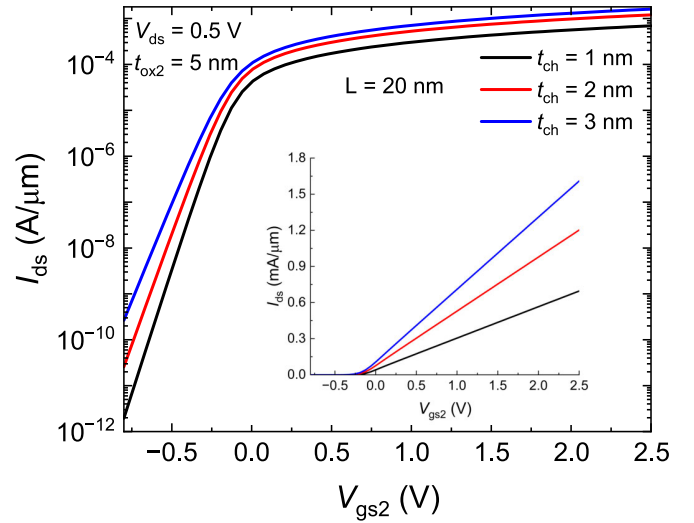


Fig. 9. Increasing channel thickness raises the OFF current due to reduced gate directional field gradient. Default parameters are taken from Fig. 1.

Fig. 9 shows the impact of channel thickness scaling on the device's OFF and ON currents. For  $L = 20 \text{ nm}$ , stronger drain electric field effects are observed, which is ideal for studying severe SCEs. Increasing channel thickness weakens gate control due to the reduced gate field gradient ( $\partial E/\partial y \downarrow$ ). The analytical model does not include scattering or mobility degradation effects. As the channel thickness increases, the gate's ability to control the channel diminishes, increasing the OFF current. However, higher channel thickness allows for greater charge density, which raises the ON current.

Fig. 10 shows the impact of trap density on the ON/OFF current characteristics. The source/drain (S/D) trap density is fixed at  $4 \times 10^{20} \text{ cm}^{-3}$ . Increasing the trap density within the channel reduces the effective barrier at equilibrium, leading to a rise in the OFF current. While the ON current also increases due to the enhanced electron density in the channel,

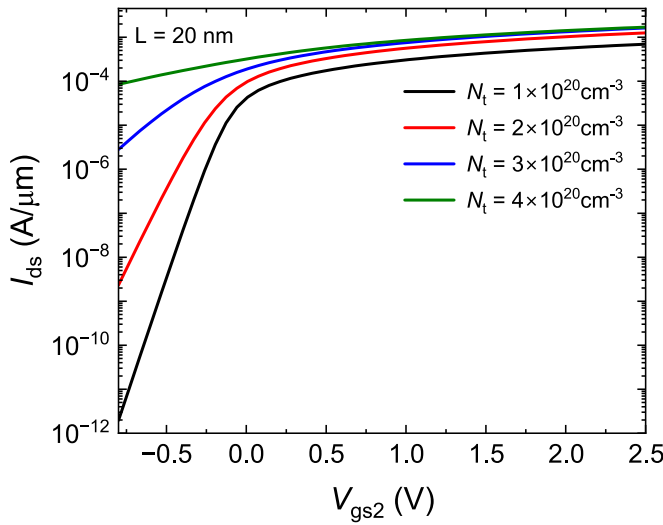


Fig. 10. Increasing channel trap density reduces the effective barrier, raising both ON and OFF currents. Default parameters are taken from Fig. 1.

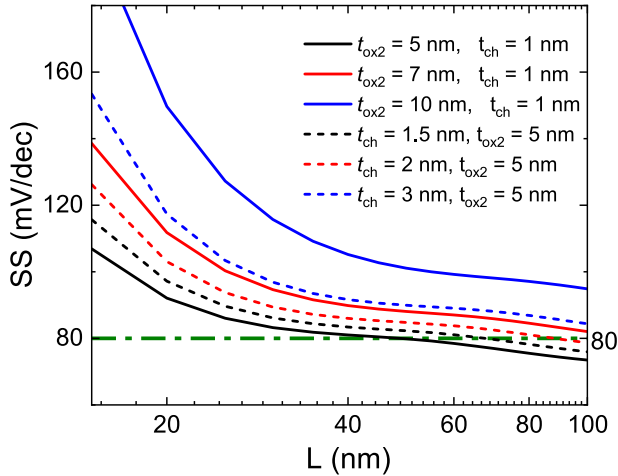


Fig. 11. SS with the channel length for the various combinations of oxide and channel thicknesses. Default parameters are taken from Fig. 1.

this improvement comes at the expense of higher OFF current levels. When the channel trap density matches that of the S/D, the barrier is almost suppressed, and the series resistances primarily limit the current.

Fig. 11 shows the SS characteristics with channel length for various oxide and channel thicknesses. The SS at  $L = 15$  nm and  $t_{ch} = 1$  nm is 107, 138, and 202 mV/decade for  $t_{ox2} = 5, 7,$  and  $10$  nm, respectively. On the other hand, the SS at  $L = 15$  nm and  $t_{ox2} = 5$  nm is 116, 126, and 153 mV/decade for  $t_{ch} = 1.5, 2,$  and  $3$  nm, respectively. Increasing the oxide thickness by  $2\times$  causes a  $\sim 95$ -mV/decade increase in the SS, while increasing the channel thickness by  $3\times$  raises the SS only by  $\sim 37$  mV/decade. Therefore, the device's SS is much more sensitive to oxide scaling than to channel thickness scaling.

Fig. 12 shows the threshold voltage roll-off plot with channel length at different oxide and channel thicknesses. As observed in the SS plot, scaling in the oxide thickness causes a significantly larger threshold voltage roll-off than the

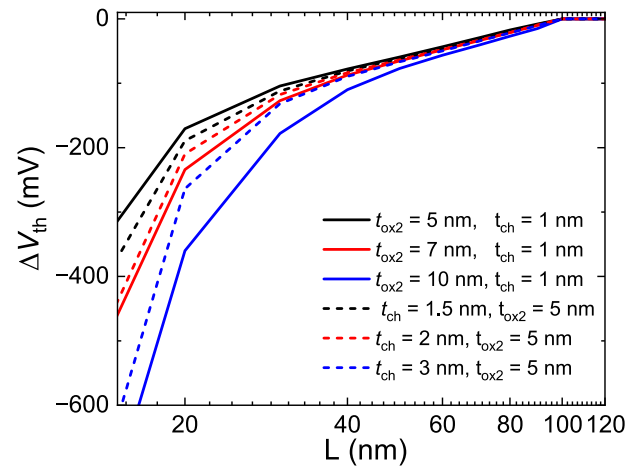


Fig. 12. Threshold voltage roll-off is more sensitive to the gate oxide scaling than the channel thickness scaling. Default parameters are taken from Fig. 1.

channel thickness scaling. From the SS and threshold voltage roll-off plots, it can be concluded that the device's short-channel characteristics are more prone to gate oxide scaling than to channel length scaling. Note that the constant current method at the  $1\text{-nA}/\mu\text{m}$  current level is used to calculate the  $V_{th}$  roll-off.

## VIII. CONCLUSION

We have developed an analytical model for  $\text{In}_2\text{O}_3$  TFTs using Green's function approach by solving 2-D Poisson's equation. Model validation against experimental and TCAD data demonstrates good agreement for both high and low drain voltages. The model accurately reflects critical phenomena such as threshold voltage roll-off, SCEs, and DIBL, with the results highlighting the tradeoffs involved in scaling gate oxide thickness, channel thickness, and channel length. Although the ON current region shows some discrepancy due to the exclusion of inversion charge density, an improved field-dependent mobility model ensures consistency in the ON region. The framework can act as a fast analytical tool to aid in the design of the device by relating its performance metrics with key geometry and material parameters.

## IX. GREEN'S FUNCTION

$$G_y^I(x, y; x', y') = \frac{2}{t_{ox1}} \sum_n \frac{\sin(k_n^I y) \sin(k_n^I y')}{k_n^I \sinh(k_n^I L)} \times \begin{cases} \sinh(k_n^I (L - x')) \sinh(k_n^I x) & 0 < x < x' \\ \sinh(k_n^I x') \sinh(k_n^I (L - x)) & x' < x < L \end{cases} \quad (57)$$

$$G_x^I(x, y; x', y') = \frac{2}{L} \sum_m \frac{\sin(k_m x) \sin(k_m x')}{k_m \cosh(k_m t_{ox1})} \begin{cases} \sinh(k_m y) \cosh(k_m (t_{ox1} - y')) & 0 < y < y' \\ \sinh(k_m y') \cosh(k_m (t_{ox1} - y)) & y' < y < t_{ox1} \end{cases} \quad (58)$$

$$G_x^{II}(x, y; x', y') = \frac{2}{L} \sum_m \frac{\sin(k_m x) \sin(k_m x')}{k_m \sinh(k_m t_{ch})}$$



$$\left\{ \begin{array}{l} \cosh(k_m(t_{ox1} - y))\cosh(k_m(t_1 - y')) \quad t_{ox1} < y < y' \\ \cosh(k_m(t_{ox1} - y'))\cosh(k_m(t_1 - y)) \quad y' < y < t_1 \end{array} \right\} \quad (59)$$

$$\begin{aligned} G_y^{II}(x, y; x', y') &= \frac{2}{t_{ch}} \sum_n \frac{\cos(k_n^{II}(t_1 - y))\cos(k_n^{II}(t_1 - y'))}{k_n^{II}\sinh(k_n^{II}L)} \\ &\times \left\{ \begin{array}{l} \sinh(k_n^{II}(L - x'))\sinh(k_n^{II}x) \quad 0 < x < x' \\ \sinh(k_n^{II}x')\sinh(k_n^{II}(L - x)) \quad x' < x < L \end{array} \right\} \quad (60) \end{aligned}$$

$$\begin{aligned} G_y^{III}(x, y; x', y') &= \frac{2}{t_{ox2}} \sum_n \frac{\sin(k_n^{III}(t_2 - y))\sin(k_n^{III}(t_2 - y'))}{k_n^{III}\sinh(k_n^{III}L)} \\ &\times \left\{ \begin{array}{l} \sinh(k_n^{III}(L - x'))\sinh(k_n^{III}x) \quad 0 < x < x' \\ \sinh(k_n^{III}x')\sinh(k_n^{III}(L - x)) \quad x' < x < L \end{array} \right\} \quad (61) \end{aligned}$$

$$\begin{aligned} G_x^{III}(x, y; x', y') &= \frac{2}{L} \sum_m \frac{\sin(k_m x)\sin(k_m x')}{k_m \cosh(k_m t_{ox2})} \\ &\times \left\{ \begin{array}{l} \cosh(k_m(t_1 - y))\sinh(k_m(t_2 - y')) \quad t_1 < y < y' \\ \cosh(k_m(t_1 - y'))\sinh(k_m(t_2 - y)) \quad y' < y < t_2 \end{array} \right\}. \quad (62) \end{aligned}$$

## REFERENCES

- [1] P. Weimer, "The TFT a new thin-film transistor," *Proc. IRE*, vol. 50, no. 6, pp. 1462–1469, Jun. 1962.
- [2] H. Kawamoto, "The history of liquid-crystal display and its industry," in *Proc. 3rd IEEE Hist. Electro-Technol. Conf. (HISTELCON)*, Sep. 2012, pp. 1–6.
- [3] E. M. C. Fortunato et al., "Fully transparent ZnO thin-film transistor produced at room temperature," *Adv. Mater.*, vol. 17, no. 5, pp. 590–594, Mar. 2005, doi: [10.1002/adma.200400368](https://doi.org/10.1002/adma.200400368).
- [4] H. S. Kim, P. D. Byrne, A. Facchetti, and T. J. Marks, "High performance solution-processed indium oxide thin-film transistors," *J. Amer. Chem. Soc.*, vol. 130, no. 38, pp. 12580–12581, Sep. 2008, doi: [10.1021/ja804262z](https://doi.org/10.1021/ja804262z).
- [5] M.-G. Kim, M. G. Kanatzidis, A. Facchetti, and T. J. Marks, "Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing," *Nature Mater.*, vol. 10, pp. 382–388, Apr. 2011, doi: [10.1038/nmat3011](https://doi.org/10.1038/nmat3011).
- [6] W. Chakraborty, B. Grisafe, H. Ye, I. Lightcap, K. Ni, and S. Datta, "BEOL compatible dual-gate ultra thin-body W-doped indium-oxide transistor with  $\text{ion} = 370\mu\text{A}/\mu\text{m}$ ,  $\text{SS} = 73\text{ mV/dec}$  and  $\text{ion}/\text{Ioff ratio} > 4 \times 10^9$ ," in *Proc. IEEE Symp. VLSI Technol.*, Jun. 2020, pp. 1–2.
- [7] T. Kamiya, K. Nomura, and H. Hosono, "Origins of high mobility and low operation voltage of amorphous oxide TFTs: Electronic structure, electron transport, defects and doping," *J. Display Technol.*, vol. 5, no. 7, pp. 273–288, Jul. 2009.
- [8] W. Tang et al., "Monolithic 3D integration of vertically stacked CMOS devices and circuits with high-mobility atomic-layer-deposited  $\text{In}_2\text{O}_3$  n-FET and polycrystalline Si p-FET: Achieving large noise margin and high voltage gain of  $134\text{ V/V}_i$ ," in *IEDM Tech. Dig.*, Dec. 2022, pp. 483–486, doi: [10.1109/IEDM45625.2022.10019410](https://doi.org/10.1109/IEDM45625.2022.10019410).
- [9] J. Zhang et al., "Back-end-of-line-compatible scaled InGaZnO transistors by atomic layer deposition," *IEEE Trans. Electron Devices*, vol. 70, no. 12, pp. 6651–6657, Dec. 2023.
- [10] P.-Y. Liao et al., "Transient thermal and electrical co-optimization of BEOL top-gated ALD  $\text{In}_2\text{O}_3$  FETs on various thermally conductive substrates including diamond," in *IEDM Tech. Dig.*, Dec. 2022, pp. 12.4.1–12.4.4.
- [11] S. Yamazaki et al., "High-performance single-crystalline  $\text{In}_2\text{O}_3$  field effect transistor toward three-dimensional large-scale integration circuits," *Commun. Mater.*, vol. 5, no. 1, p. 184, Sep. 2024, doi: [10.1038/s43246-024-00625-x](https://doi.org/10.1038/s43246-024-00625-x).
- [12] P. D. C. King, T. D. Veal, D. J. Payne, A. Bourlange, R. G. Egdell, and C. F. McConville, "Surface electron accumulation and the charge neutrality level in  $\text{In}_2\text{O}_3$ ," *Phys. Rev. Lett.*, vol. 101, no. 11, Sep. 2008, Art. no. 116808, doi: [10.1103/physrevlett.101.116808](https://doi.org/10.1103/physrevlett.101.116808).
- [13] L. Liu et al., "Theoretical study of oxygen-vacancy distribution in  $\text{In}_2\text{O}_3$ ," *J. Phys. Chem. C*, vol. 125, no. 13, pp. 7077–7085, Apr. 2021, doi: [10.1021/acs.jpcc.1c01462](https://doi.org/10.1021/acs.jpcc.1c01462).
- [14] J. H. W. De Wit, G. Van Unen, and M. Lahey, "Electron concentration and mobility in  $\text{In}_2\text{O}_3$ ," *J. Phys. Chem. Solids*, vol. 38, no. 8, pp. 819–824, Jan. 1977, doi: [10.1016/0022-3697\(77\)90117-2](https://doi.org/10.1016/0022-3697(77)90117-2).
- [15] M. Shur, M. Hack, and J. G. Shaw, "A new analytic model for amorphous silicon thin-film transistors," *J. Appl. Phys.*, vol. 66, no. 7, pp. 3371–3380, Oct. 1989, doi: [10.1063/1.344481](https://doi.org/10.1063/1.344481).
- [16] M. D. Jacunski, M. S. Shur, A. A. Owusu, T. Ytterdal, M. Hack, and B. Iniguez, "A short-channel DC SPICE model for polysilicon thin-film transistors including temperature effects," *IEEE Trans. Electron Devices*, vol. 46, no. 6, pp. 1146–1158, Jun. 1999.
- [17] H. Tsuji et al., "A new surface potential based poly-Si TFT model for circuit simulation," in *IEDM Tech. Dig.*, San Francisco, CA, USA, Dec. 2006, pp. 1–4.
- [18] Y. Hernández-Barrios, A. Cerdeira, M. Estrada, and B. Iniguez, "Analytical current-voltage model for double-gate a-IGZO TFTs with symmetric structure for above threshold," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 1980–1986, May 2020.
- [19] W. Deng, J. Huang, X. Ma, and T. Ning, "An explicit surface-potential-based model for amorphous IGZO thin-film transistors including both tail and deep states," *IEEE Electron Device Lett.*, vol. 35, no. 1, pp. 78–80, Jan. 2014.
- [20] Z. Zong, L. Li, J. Jang, N. Lu, and M. Liu, "Analytical surface-potential compact model for amorphous-IGZO thin-film transistors," *J. Appl. Phys.*, vol. 117, no. 21, Jun. 2015, Art. no. 215705, doi: [10.1063/1.4922181](https://doi.org/10.1063/1.4922181).
- [21] M. Ghittorelli, F. Torricelli, L. Colalongo, and Z. M. Kovács-Vajna, "Accurate analytical physical modeling of amorphous InGaZnO thin-film transistors accounting for trapped and free charges," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4105–4112, Dec. 2014.
- [22] G. Pahwa, S. Salahuddin, and C. Hu, "An all-region BSIM thin-film transistor model for display and BEOL 3-D integration applications," *IEEE Trans. Electron Devices*, vol. 71, no. 8, pp. 4701–4709, Aug. 2024.
- [23] J. Pruefer et al., "Compact modeling of short-channel effects in staggered organic thin-film transistors," *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 5082–5090, Nov. 2020, doi: [10.1109/TED.2020.3021368](https://doi.org/10.1109/TED.2020.3021368).
- [24] F. Torricelli, Z. M. Kovács-Vajna, and L. Colalongo, "A charge-based OTFT model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 56, no. 1, pp. 20–30, Jan. 2009, doi: [10.1109/TED.2008.2007717](https://doi.org/10.1109/TED.2008.2007717).
- [25] X. Liang and Y. Taur, "A 2-D analytical solution for SCEs in DG MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1385–1391, Sep. 2004, doi: [10.1109/TED.2004.832707](https://doi.org/10.1109/TED.2004.832707).
- [26] N. Pandey, H.-H. Lin, A. Nandi, and Y. Taur, "Modeling of short-channel effects in DG MOSFETs: Green's function method versus scale length model," *IEEE Trans. Electron Devices*, vol. 65, no. 8, pp. 3112–3119, Aug. 2018, doi: [10.1109/TED.2018.2845875](https://doi.org/10.1109/TED.2018.2845875).
- [27] Q. Xie, J. Xu, and Y. Taur, "Review and critique of analytic models of MOSFET short-channel effects in subthreshold," *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1569–1579, Jun. 2012.
- [28] N. Pandey and Y. S. Chauhan, "Dynamics and modeling of multidomains in ferroelectric tunnel junction—Part I: Mathematical framework," *IEEE Trans. Electron Devices*, vol. 69, no. 12, pp. 7147–7155, Dec. 2022.
- [29] B. G. Streetman and S. Banerjee, *Solid State Electronic Devices*, vol. 4. Upper Saddle River, NJ, USA: Prentice-Hall, 2000.
- [30] W. J. Chang, M. P. Houn, and Y. H. Wang, "Simulation of stress-induced leakage current in silicon dioxides: A modified trap-assisted tunneling model considering Gaussian-distributed traps and electron energy loss," *J. Appl. Phys.*, vol. 89, no. 11, pp. 6285–6293, Jun. 2001, doi: [10.1063/1.1367399](https://doi.org/10.1063/1.1367399).
- [31] H. S. Bennett, M. Gaitan, P. Roitman, T. J. Russell, and J. S. Suehle, "Modeling MOS capacitors to extract Si— $\text{SiO}_2$  interface trap densities in the presence of arbitrary doping profiles," *IEEE Trans. Electron Devices*, vol. ED-33, no. 6, pp. 759–765, Jun. 1986.
- [32] J. D. Jackson, *Electrodynamics, Classical*. Hoboken, NJ, USA: Wiley, 2003, doi: [10.1002/3527600434.eap109](https://doi.org/10.1002/3527600434.eap109).
- [33] N. Pandey, "Modeling of ferroelectric memories and transistors including multi-domain effects," Ph.D. dissertation, Dept. Elect. Eng., Indian Inst. Technol. Kanpur, Kanpur, India, 2023, doi: [10.13140/RG.2.2.22419.45603](https://doi.org/10.13140/RG.2.2.22419.45603).